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DE FR GB NL(71) Applicant: TEKTRONIX, INC.
Howard Vollum Park 14150 S.W. Karl Braun
Drive P.O. Box 500
Beaverton Oregon 97077(US)(72) Inventor: Auel, Kendall Poul
12370 Wilsonville Road
Wilsonville Oregon 97070(US)
Inventor: Delwiche, James Anthony
20898 S.W. 104th Avenue
Tualatin Oregon 97062(US)(74) Representative: Liesegang, Roland, Dr.-Ing.
FORRESTER & BOEHMERT
Widenmayerstrasse 4
D-8000 München 22(DE)

(54) Double buffered graphics design system.

(57) A graphic display system comprises a video display controller including two similar frame buffer memories for alternatively receiving and storing incoming pixel data and for periodically refreshing a display on a screen selectively in accordance with pixel data stored by either one of the two frame buffer memories. While the video display controller periodically refreshes the screen display in accordance with the pixel data stored in a first of the frame buffer memories, incoming pixel data is stored in the second frame buffer memory. The video display controller begins periodically refreshing the screen display in accordance with the pixel data stored in the second frame buffer memory. Updated pixel data stored in the second frame buffer memory is then copied into the first frame buffer memory.

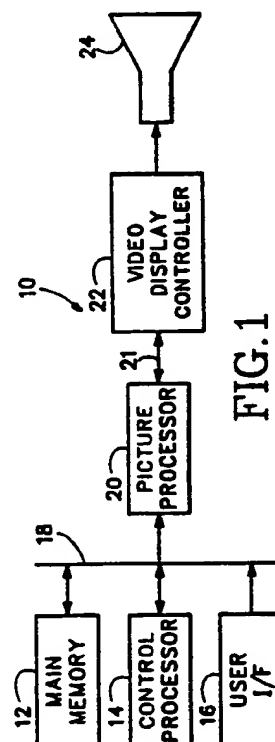


FIG. 1

DOUBLE BUFFERED GRAPHICS DISPLAY SYSTEM

Background of the Invention

The present invention relates in general to graphics display systems and in particular to a system utilizing two frame buffer memories to alternately control a graphics display.

Graphics display systems often characterize a graphics design in the form of a "display list" stored in a random access memory, the display list comprising a set of instructions for creating pixel data from which a pixel-based graphics display can be produced on a cathode ray tube (CRT) screen. When the display list is modified to reflect a change in the graphic design, a picture processor reads the display list out of the main memory, executes the instructions therein to generate the pixel data, and then transmits the pixel data to a video display controller that controls the display on the CRT. The video display controller includes a frame buffer memory for storing the pixel data and includes refresh circuitry for periodically refreshing the graphics display in accordance with the pixel data.

Display lists typically include information from which may be determined the color and/or intensity of every pixel included in the graphics design but do not include information relative to individual pixels that are to remain at a background color. As it begins processing a display list, the picture processor initially commands video display controller to clear the frame buffer memory so as to set all screen pixels to the background color on the next screen refresh cycle. Thereafter, the picture processor processes the display list and transmits pixel data to the video display controller for storage in the frame buffer memory. The pixel data tells the video display controller to set certain of the screen pixels to other than the background color. Following the next screen refresh cycle, all or a portion of the graphic design appears on the screen, depending on how much of the display list was processed. Many picture processors can process a display list defining a relatively simple design fast enough that the display will be fully redrawn between two refresh operations. More complex designs may require two or more refresh cycles for a complete screen redraw.

Some systems permit a user to relocate a graphic object within a graphic design by using a cursor to select the graphic object when displayed on a screen, and then dragging the cursor across the screen to a desired position. Such a system continuously modifies the display list and causes

the picture processor to process the display list several times as the user moves the cursor across the screen so that the object is displayed at several successive locations on the screen, thereby giving the illusion that the object is moving across the screen with the cursor. However, each time the display is redrawn, it is initially set to the background color ("erased"), and a user perceives a noticeable and distracting flicker in the display as the display is repetitively erased and then redrawn.

Summary of the Invention

A computer graphics system includes a picture processor for generating pixel data in response to a display list defining a graphics design, the pixel data in turn defining a pixel map indicating colors and/or other display attributes of various pixels on a cathode ray tube (CRT) screen. In accordance with one aspect of the invention, the graphics system further includes a video display controller having similar first and second frame buffer memories, each for alternatively receiving and storing pixel data generated by the picture processor so as to provide separate pixel maps of the graphics display. Refresh circuitry within the video display controller refreshes the video display selectively in accordance with pixel data stored by either one of the first and second frame buffer memories.

In accordance with another aspect of the invention, while the refresh circuitry refreshes the CRT screen display in accordance with the pixel data stored in one of the frame buffer memories, pixel data generated by the picture processor in response to a changed display list is stored in the other frame buffer memory. When the pixel data in the other frame buffer memory has been fully updated to reflect the change in the display list, the refresh circuitry begins using the pixel data stored in the second frame buffer memory to control screen refresh. Thus, following a change in the display list, the display continues unchanged until the pixel data in the frame buffer memory not controlling screen refresh is fully updated to reflect the change. At that point the display is completely updated in one refresh cycle in accordance with the updated pixel data and a viewer perceives a complete, instantaneous change in the graphics display. The use of double frame buffer memories eliminates flicker in the display as typically occurs in systems of the prior art having a single frame buffer memory wherein display is temporarily erased between updates.

In accordance with a further aspect of the invention, the video display controller also includes means for rapidly copying selected portions of the pixel data from each frame buffer memory to the other. After a frame buffer memory is updated in response to a change in a display list, and after it begins to control screen refresh, contents of that memory are copied into the other frame buffer memory so that the pixel data stored in both frame buffer memories reflect the current state of the display list. When multiple display lists define separate graphic displays ("views"), portions of which may be simultaneously shown in separate windows on the same CRT screen, the picture processor processes only those display lists relating to views that are changed and only those portions of the frame buffer memory not currently controlling the screen refresh are erased and rewritten. Since it is not necessary to process all of the display lists defining currently displayed views, display update speed is improved.

It is accordingly an object of the invention to provide a graphics system wherein graphic displays produced on a CRT screen in accordance with one or more display lists are completely updated during a single screen refresh cycle in response to a change in the display list without temporally erasing the screen.

It is another object of the invention to provide an improved graphics system wherein graphic displays produced on a CRT screen in accordance with display lists are rapidly updated in response to changes in the display lists.

The subject matter of the present invention is particularly pointed out and distinctly claimed in the concluding portion of this specification. However, both the organization and method of operation of the invention, together with further advantages and objects thereof, may best be understood by reference to the following description taken in connection with accompanying drawings wherein like reference characters refer to like elements.

Description of the Drawings

FIG. 1 is a block diagram of a video graphics system in accordance with the present invention;

FIG. 2 is a block diagram of the video display controller of FIG. 1;

FIG. 3 is a block diagram of a frame buffer memory controller of FIG. 2; and

FIG. 4 is state diagram illustrating a method of operation of the video display controller of FIG. 1 in accordance with the present invention.

Detailed Description of the Invention

With reference to FIG. 1, a graphics display system 10 comprises a main memory 12 for storing display lists, each display list comprising a set of instructions for producing a graphic display on a screen of a cathode ray tube 24. A display list may be changed by a control processor 14 under control of graphics software that may also be stored in memory 12, the display list being altered to change the graphic design that it represents in response to user commands supplied to control processor 14 through a keyboard, mouse and/or other input device via user interface circuitry 16. Main memory 12, processor 14, and user interface circuit 16 are interconnected through a computer bus 18 which is also connected to a picture processor 20. When a user commands the control processor 14 to change a display list, the control processor 14 sequentially transfers the changed display list out of memory 12 to picture processor 20 via bus 18. Picture processor 20 processes the display list to generate pixel data, addresses and control signals which are transmitted via a local bus 21 to a video display controller 22. The video display controller stores the pixel data that it receives and uses the stored pixel data to control video signals that refresh a display produced on the screen of cathode ray tube (CRT) 24.

The control processor can also send commands to the video display controller 22 via picture processor 20 and local bus 21, which commands cause the video display controller to read out pixel data stored therein onto the local bus for transmission back to main memory 12 via local bus 21, picture processor 20 and computer bus 18. This read operation is useful when the display on CRT 24 comprises multiple overlapping graphic windows. When a portion of one window is to be temporarily covered by another, pixel data defining the covered portion may be read out of the video display controller and temporarily store in main memory 12. After the covered window is uncovered, the pixel data in main memory 12 is transmitted through picture processor 20 and back into display controller 22 for storage therein. Since the pixel data is already in the appropriate form, it is not necessary for picture processor 20 to spend as much time processing it as if the screen were updated from a display list. Thus, screen update speed is improved.

In accordance with the invention, the video display controller 22 of FIG. 1, shown in more detailed block diagram form in FIG. 2, comprises two frame buffer memory controllers A and B (devices 26 and 28), a bus arbitrator 30 and a control register 32, all connected to the local bus

21. Frame buffer memory controller A receives pixel data and control signals from the picture processor via local bus 21 and stores the pixel data in a frame buffer memory A (device 34). Similarly, frame buffer memory controller B receives pixel data and control signals via local bus 21 and stores the pixel data in a frame buffer memory B (device 36). Frame buffer memory controllers A and B can also read pixel data out of frame buffer memories 34 and 36, respectively, and transmit the pixel data back through bus 21. Bus arbitrator 30 controls access to bus 21 by frame buffer memory controllers A and B and determines which frame buffer memory controller receives incoming data and control signals on bus 21.

Pixel data words read out of frame buffer memories A and B are also provided as inputs to a multiplexer 38 which passes a selected one of the words at its input to conventional color map and video driver circuits 40. Circuits 40 generate signals for controlling electron beams of CRT 24 of FIG. 1 during refresh operations so as to produce a display on the screen of CRT 24 in accordance with the pixel data output of multiplexer 38. Frame buffer memory controllers A and B transmit address and control signals to frame buffer memories 34 and 36 when CRT 24 is to be refreshed, thereby causing all of the data in the frame buffer memories to be read out in sequence and supplied to multiplexer 38. Multiplexer 38 thus selects which of the frame buffer memories A or B is to supply pixel data for controlling CRT screen refresh. The switching state of multiplexer 38 is in turn controlled by a bit stored in control register 32 by signals transmitted thereto from picture processor 20 of FIG. 1 via local bus 21 on completion of display list processing.

Control processor 14 of FIG. 1 keeps track of the switching state of multiplexer 38 of FIG. 2 so that it can determine which frame buffer memory A or B is currently supplying pixel data controlling screen refresh operations. When a display list is sent to the picture processor 20, control processor 14 transmits a command to the picture processor telling it to set to a particular state a control bit included with any pixel data subsequently sent to the video display controller 22. The state of the control bit tells the bus arbitrator 30 of FIG. 2 whether frame buffer memory controller A or B is to receive the pixel data on the local bus 21, and the bus arbitrator input enables the indicated frame buffer memory controller.

In accordance with the invention, when the pixel data stored in frame buffer memory A is used to control screen refresh, pixel data generated by the picture processor 20 in response to a changed display list is written into frame buffer memory B. When the display list is fully processed, and the

resulting pixel data stored in frame buffer memory B, the control processor 14 sends a command to the video display controller 22 via picture processor 20 which command causes control register 32 to switch the state of multiplexer 30. Thereafter, screen refresh is controlled by the pixel data stored by frame buffer memory B and any additional pixel data generated by the picture processor 20 in response to a subsequently changed display list is written into the frame buffer memory A. When the pixel data in frame buffer memory A has been updated, control of refresh operation is switched back to memory A. Thus, following a change in a display list, the display on CRT 24 of FIG. 1 continues unchanged until the pixel data in the particular frame buffer memory A or B that is not currently controlling screen refresh is fully updated to reflect the display list change. The state of multiplexer 38 is then switched and the display on CRT 24 is updated during the next refresh cycle.

In display systems of the prior art utilizing a single frame buffer memory, the frame buffer memory is cleared and then rewritten with new pixel data in response to each change in a display list. When the frame buffer memory is cleared, the screen is erased before the updated display appears. The temporary screen erasing between display updates causes the display to exhibit a distracting flicker when display lists are changed more or less continuously. The use of the double frame buffer memories permits the display to be changed from one state to another in an apparently instantaneous fashion, a short time after each change in a display list, without having to erase the screen between display updates. Thus, the graphic display system of the present invention does not produce a flickering display in response to substantially continuous display list changes as do graphic display systems of the prior art.

After, for example frame buffer memory B is updated in response to a change in a display list, and after it subsequently begins to control screen refresh, pixel data stored in frame buffer memory B is copied into frame buffer memory A so that pixel data stored in both frame buffer memories reflect the current display lists. Multiple display lists stored in memory 12 may define separate graphic displays, views of which may be simultaneously shown in separate windows on the same CRT screen. Since the pixel data stored in both frame buffer memories is current, except for the data associated with the particular window to be changed, the picture processor 20 processes only the display list relating to that particular window and sends only the portion of the pixel data defining the changed window to the video display controller 22 for storage in one of its frame buffer memories. Since it is not necessary to process all

of the display lists defining currently displayed views, the display may be updated quickly, particularly when the window being updated is small in relation to the total available screen area. Thus, by providing the video display controller 22 with the ability to copy pixel data from one frame buffer memory to the other, the amount of display list processing by picture processor 20 is minimized, thereby increasing the speed with which the displays can be updated, particularly when the display includes multiple windows controlled by separate display lists.

FIG. 3 is a block diagram showing frame buffer memory controller A of FIG. 2 in more detail. (Frame buffer memory controller B is similar.) Frame buffer memory controller A includes a buffer 50 for receiving data and control signals conveyed on local bus 21 and for forwarding the signals to an X address counter 52, a Y address counter 54, a multiplexer 56 and a control register 58. Buffer 50 is output enabled by a signal from the bus arbitrator 30 of FIG. 2.

When writing data into frame buffer memory A of FIG. 2, picture processor 22 of FIG. 1 sends sequences of pixel data to frame buffer memory controller A via local bus 21, each pixel data sequence being preceded by data conveying a starting address at which the first pixel data element of the sequence is to be stored and additional control bits which are stored in control register 32. Frame buffer memory addressing is organized into a two-dimensional X,Y array wherein each address has an X and a Y component. The display on the screen of CRT 24 of FIG. 1 is formed by a corresponding X,Y array of pixels, and the pixel data stored at address (X,Y) controls display attributes of a pixel at a point (X,Y) on the screen. The X component of the starting address is loaded into X counter 52 and the Y component of the starting address is loaded into Y address counter 54. Counters 52 and 54 may count up or down from the starting address X and Y components in response to count enabling signals produced by a bus control state machine 59. State machine 59 is clocked by a control signal on bus 21 and receives as input the control data bits stored in control register 58. The address control data indicates whether each address counter 52 and 54 is to count up or down, or not at all. Each sequence of pixel data includes one or more pixel data words representing a single pixel or a line of several pixels that may extend in any direction on the screen from the pixel at point (X,Y). The direction of the count of each address counter 52, 54 controls the manner in which the frame buffer memory address is changed after each pixel data word of a sequence is stored. The X and Y address components stored in counters 52 and 54 are incremented or decremented in accor-

dance with the control bits in register 58 such that the stored pixel data controls a line of pixels on the screen starting at the designated starting point (X,Y) and extending in the appropriate direction.

The address output of address counters 52 and 54 and the pixel data output of multiplexer 56 are initially stored in a register 60 and then transferred through a latch 62 to a multistage first-in-first-out (FIFO) buffer 64. The address passes out of FIFO buffer 64, through a multiplexer 70 and a buffer 72, to address inputs of the frame buffer memory. The pixel data passes from FIFO buffer 64 and into an input of a logic unit 66. Logic unit 66 may be set to pass the pixel data unchanged through a buffer 68 and into address inputs of the frame buffer memory. Logic unit 66 may alternatively be set to produce a logical or arithmetic combination (AND, XOR, sum, etc.) of the pixel data output of FIFO buffer 64 and data previously read from the frame buffer memory to supply pixel data to be transmitted back into the frame buffer memory via buffer 68. Logic unit 66 permits incoming images to be superimposed over, or otherwise combined with, existing images on the screen.

Control bits, conveyed on bus 21 with the pixel data and passed therewith through FIFO buffer 64, indicate whether valid data is stored in the FIFO buffer and whether a read or write operation is to be carried out, and also indicate the type of logical or arithmetic operation to be performed by logic unit 66, if any. These control bits, when shifted out of FIFO buffer 64, are supplied to inputs of a memory control state machine 74 that controls the switching state of multiplexer 70, the nature of operations of logic unit 66, and the output enabling of buffer 68. Memory control state machine also controls a read/write enabling signal transmitted to the frame buffer memory via a buffer 76.

Thus, to write a pixel data sequence into the frame buffer memory, the starting address is loaded into X and Y address counters 52 and 54, address incrementing control bits are loaded into control register 58, and then the data sequence, along with control bits on bus 21 and the address generated by address counters 52 and 54 are sequenced through register 60, latch 62 and FIFO buffer 64 under control of state machine 59. As the data, address and control bits emerge from FIFO buffer 64 the address bits address the frame buffer memory via multiplexer 70 and buffer 72, the pixel data is supplied to the memory via logic unit 66 and buffer 68, and the control data is supplied to state machine 74 which supplies the necessary signal to control multiplexer 70, logic unit 66, and buffer 68.

Pixel data may also be read out of the frame buffer memory, and transferred back to the picture processor via local bus 21. As in a write operation,

the picture processor places on bus 21 a starting X,Y address and control bits indicating count directions for address counters 52 and 54. The starting address is loaded into address counters 52 and 54. The picture processor then places on bus 21 a sequence of "null" pixel data words along with a read/write bit set to indicate a read operation. When the null data words and accompanying control bits and the addresses generated by address counters 52 and 54 pass through FIFO buffer 64, memory control state machine 74 recognizes from the incoming read/write bit that a read operation is contemplated and transmits a read control signal to the frame buffer memory so that the memory will read out pixel data stored at the address supplied through buffer 72. As the data is read out, it passes through a buffer 82 and a pair of latches 84 and 86 to an input of a read data register 88. On the next local bus 21 cycle, the data is stored in register 88 and then transmitted through a buffer 94 to bus 21. Latches 84 and 86 are controlled by signals from state machine 74 in response to the read/write control bit output of FIFO buffer 64. Read data register 88 is controlled by state machine 59 in response to a control signal on bus 21. Buffer 94 is output enabled by bus arbitrator 30 of FIG. 2.

The data output of register 88 is also supplied to an input of multiplexer 56 so that it may subsequently pass through register 60, latch 62 and FIFO buffer 64 for storage at another location in the frame buffer memory. The feedback path provided by multiplexer 56 permits data to be rapidly copied from one storage location in the frame buffer memory to another. The data read out of the frame buffer memory is also latched onto an input of logic unit 66 so logic unit 66 may selectively combine the data with incoming pixel data from FIFO buffer 64.

Pixel data may also be rapidly copied from either one of the frame buffer memories A and B into the other by using a read operation followed by a write operation. For example, with reference to FIGS. 2 and 3, data may be read out of frame buffer memory A, stored temporarily by picture processor 20, and then written back into frame buffer memory A.

To maintain the display on the CRT screen, the display is periodically refreshed. The frame buffer memory, being a dynamic random access memory, must also be periodically refreshed. Refresh counters 92, responding to externally generated synchronizing signals, address the frame buffer memory during memory and screen refresh operations using address signals R.A. or S.A., respectively, provided to the frame buffer memory address terminals through multiplexer 70 and buffer 72. State machine 74, in response to a synchronizing signal from counters 92, suspends any other

memory read/or write access operation in progress, appropriately sets the state of multiplexer 70, and sets its read/write control signal output to the appropriate state so that the frame buffer memory is read accessed during the refresh operation.

FIG. 4 is a state diagram showing an algorithm implemented by control processor 14 with respect to each view that it maintains on the CRT screen. In FIG. 4, the term "front" refers to the particular one of frame buffer memories A or B that is currently controlling screen refresh and the term "back" refers to the other frame buffer memory. When the control processor 14 of FIG. 1 initiates an update of a display list associated with a view displayed on the CRT screen, the processor designates the view as being in a state A (block 102 of FIG. 4) wherein the pixel data associated with the view in neither the front nor back frame buffer memories is "current" insofar as the pixel data in neither memory represents the view in accordance with current state of the display list that defines the view. When a view is in state A the system continues to refresh the screen in accordance with the pixel data stored in the front frame buffer memory while the control processor transmits the display list to the picture processor. The picture processor processes the changed display list and transmits the resulting pixel data to the back frame buffer memory for storage therein. The control processor then alters the switching state of multiplexer 38 of FIG. 2, thereby "swapping" the front and back frame buffer memories so that the memory containing the newly processed pixel data is now the front frame buffer memory supplying pixel output to the color map and driver circuits 40 and the other frame buffer memory is now the back frame buffer memory.

The view that has been updated is thereupon assigned to a state B (block 104) wherein the front frame buffer memory is identified as being current for that view, insofar as it includes the last processed pixel data defining the view, but the back frame buffer memory is not current. If the display list associated with the view is still being updated, then the system redesignates the view as being in state A because the front frame buffer memory is no longer current. However, if the display list is not still being updated, then the last processed pixel data associated with the view is copied out of the front frame buffer memory and into the back frame buffer memory so that both buffer memories are current, and the state designation of the view is changed from state B to a state C (block 106). The view remains in state C until such time as the processor initiates another update of the display list. At that point the view is again redesignated as being in state A.

Control processor 14 of FIG. 1 is suitably of the

type, that implements multiple processes on a time sharing basis. The following pseudocode listing illustrates programming of control processor 14 for implementing a process for controlling the timing of updating of pixel data in the back frame buffer memory, of front-to-back frame buffer memory swapping, and of copying pixel data from the front to the back frame buffer memory:

```

1 Process Update_Display
2 reset_timer (frame interval)
3 repeat
4 if (any view is in state A)
5 for (all views in state B)
6 pixel_copy (viewport, front to back)
7 set view to state C
8 for (all views in state A)
9 renew_view (back)
10 set view to state B
11 wait until timer expires
12 swap buffer memories
13 reset_time (frame interval)
14 else (no view is in state A)
15 wait until a view enters state A
16 forever

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Line 1 is the title of the process. In line 2, a software-implemented timer is set with a frame interval time provided when the subroutine is initially called. The frame interval time is a minimum time period during which the control processor will wait before swapping the front and back frame buffer memories. Lines 3 and 16 constitute a command to repeatedly execute lines 4 through 15 until the processor is reset. Line 4 is a command to implement lines 5-13 if any view is in state A (i.e., if a display list associated with any view has been altered since the front and back frame buffer memories were last swapped). Line 5 is a command to execute lines 6 and 7 with respect to each view that is in state B (i.e., for each view that is current in the front frame buffer memory but not current in the back frame buffer memory). In line 6, the "viewport" (i.e., the pixel data defining the portion of the view that is displayed) is copied from the front to the back frame buffer memory, and in line 7, the view is redesignated as being in state C wherein both front and back frame buffer memories are current. Line 8 is a command to execute lines 9 and 10 with respect to each view that is in state A and in line 9, the display list associated with the view is processed and stored in the back frame buffer memory. In line 10, the view is redesignated as being in state B. In line 11, the control processor suspends execution of the process until the timer indicates that the frame interval time has expired, if such time has not already expired. (In the meantime the processor may continue to execute other processes wherein the display lists

may be changed and views are redesignated as being in state A.) Then in line 12, the control processor initiates swapping of the front and back frame buffer memories. In line 13 the timer is reset to the frame interval time. Line 14 is a command to execute line 15 only if no view is in state A, and line 15 is a command to wait until a view enters state A.

Thus, in accordance with the invention, a graphic display system comprises a video display controller including two similar frame buffer memories for alternatively receiving and storing pixel data and for producing a display on a CRT screen selectively in accordance with pixel data stored by either one of the two frame buffer memories. A method of operation of the display controller has been described wherein while the video display controller periodically refreshes the CRT screen display in accordance with the pixel data stored in a first of the frame buffer memories, newly processed pixel data is stored in the second frame buffer memory. Thereafter, the video display controller begins refreshing the CRT screen display in accordance with the pixel data stored in the second frame buffer memory. Updated pixel data stored in the second frame buffer memory is then copied into the first frame buffer memory.

While a preferred embodiment of the present invention has been shown and described, it will be apparent to those skilled in the art that many changes and modifications may be made without departing from the invention in its broader aspects. The appended claims are therefore intended to cover all such changes and modifications as fall within the true spirit and scope of the invention.

Claims

1. In a graphic display system for producing a graphic display in response to incoming pixel data defining the graphic display, the graphic display system comprising a screen for providing a display and a display controller, including two frame buffer memories, for alternatively receiving and storing the incoming pixel data, for selectively copying pixel data stored in either one of the frame buffer memories to another of the frame buffer memories, and for selectively controlling the display on the screen in accordance with pixel data stored by either one of the two frame buffer memories, a method of operation for the display controller comprising the steps of:

a. controlling the screen display in accordance with the pixel data stored in a first of the frame buffer memories,

b. storing incoming pixel data in the second frame buffer memory, and

c. controlling the screen display in accordance with the pixel data stored in the second frame buffer memory upon completion of step b.

2. The method of claim 1 further comprising the step of copying the pixel data stored in the second frame buffer memory in step b into the first frame buffer memory.

3. For a graphic display system including picture processing means for generating pixel data defining a graphic display, memory means for storing and reading out first and second sets of pixel data, each of the first and second pixel data defining graphic displays, and display means for displaying a graphic display defined in accordance with pixel data read out of the memory means, a method of operation comprising the steps of:

a. reading the first set of pixel data out of the memory means and providing the read out first set of pixel data to the display means so that the display means displays a graphic display defined in accordance with the first set of pixel data;

b. altering the second set of pixel data in accordance with the pixel data generated by the picture processing means;

c. periodically repeating step a until performance of step b is complete; and

d. reading the second set of pixel data out of the memory means and providing the read out second set of pixel data to the display means so that the display means displays a graphic display defined in accordance with the second set of pixel data.

4. The method of claim 3 comprising the further steps of:

e. reading pixel data of the second set of pixel data out of the memory means after performance of step d is complete; and

f. altering the first set of pixel data in accordance with the pixel data read out of the memory means in step e.

5. For a graphic display system comprising means for storing multiple display lists, each display list representing a separate graphic design, picture processing means for processing ones of the display lists to produce pixel data defining a graphic display in accordance with the graphic design represented by the processed display list, memory means for storing and reading out first and second sets of pixel data, each of the first and second pixel data defining a plurality of graphic displays, and display means for simultaneously displaying a plurality of graphic displays defined in accordance pixel data read out of the memory means, a method of operation comprising the steps of:

a. reading the first set of pixel data out of the memory means and providing the read out first set of pixel data to the display means so that the display means displays a plurality of graphic displays defined in accordance with the first set of pixel data;

b. processing one of the display lists to produce pixel data defining a particular display and altering the second set of pixel data in accordance with the pixel data generated by the picture processing means so that the plurality of displays defined by the second set of pixel data includes the particular display;

c. repeating step a until performance of step b is complete; and

d. reading the second set of pixel data out of the memory means and providing the read out second set of pixel data to the display means so that the display means displays the plurality of graphic displays including the particular display defined in accordance with the second set of pixel data.

6. The method of claim 5 comprising the further steps of:

e. reading pixel data of the second set of pixel data defining the particular display out of the memory means after performance of step c is complete; and

f. altering the first set of pixel data in accordance with the pixel data read out of the memory means in step e so that the second set of pixel data also defines the particular display.

7. A graphic display system for producing a graphic display in response to incoming pixel data defining the graphic display comprising:

a screen for providing a display; and a display controller comprising two frame buffer memories for alternatively receiving and storing the incoming pixel data and comprising means for controlling the display on the screen selectively in accordance with pixel data stored by either one of the two frame buffer memories.

8. A graphic display system responsive to input pixel data and control data for producing a graphic display, the system comprising:

memory means for storing and reading out first and second sets of pixel data, each of the first and second sets of pixel data separately defining a graphic display; and

memory control means for receiving the input pixel data and control data, for writing the input pixel data into the memory means thereby altering in accordance with the input pixel data selectively either one of the first and second sets of pixel data, and for periodically reading out selectively either one of the first and second sets of pixel data,

selection of the pixel set altered and of the pixel set read out being made in accordance with the control data.

9. The system in accordance with claim 8 further comprising display means for receiving pixel data sets read out of the memory means and for controlling a graphic display in accordance with each pixel data set received.

10. A graphic display system, responsive to input pixel data and control data, for producing a graphic display, the apparatus comprising: memory means for storing and reading out first and second sets of pixel data, each of the first and second sets of pixel data separately defining a graphic display; and memory control means for receiving the input pixel data and control data, for writing the input pixel data into the memory means thereby altering in accordance with the input pixel data a selected one of the first and second sets of pixel data, for reading out of the memory means a selected one of the first and second sets of pixel data, for reading selected first pixel data of the first pixel data set and writing the first pixel data back into the memory means, thereby altering the second pixel data set in accordance with the first pixel data, and for reading selected second pixel data of the second pixel data set and writing the second pixel data back into the memory means, thereby altering the first pixel data set in accordance with the second pixel data, selections of the one pixel set altered, of the one pixel set read out, of the first pixel data and of the second pixel data being made in accordance with the control data.

11. The system in accordance with claim 10 further comprising display means for receiving pixel data sets read out of the memory means and for controlling a graphic display in accordance with each pixel data set received.

12. A graphic display system comprising: a screen for presenting a graphic display; storage means for storing and reading out a display list defining pixel and control data, the pixel data defining a graphic display to be presented on the screen; picture processing means for receiving the display list read out of the storage means and for generating the pixel and control data defined by the display list; memory means for storing and reading out first and second sets of pixel data, each of the first and second sets of pixel data defining graphic displays to be presented on the screen; memory control means for receiving the pixel and control data produced by the picture processing means, for writing the received pixel data into the memory means thereby altering in accordance with the pixel data produced by the picture processing

means one of the first and second sets of pixel data selected in accordance with the control data, and for causing the memory means to read out one of the first and second sets of pixel data selected in accordance with the control data; and display control means for controlling the screen so as to produce thereon a graphic display defined in accordance with the selected set of pixel data read out of the memory means.

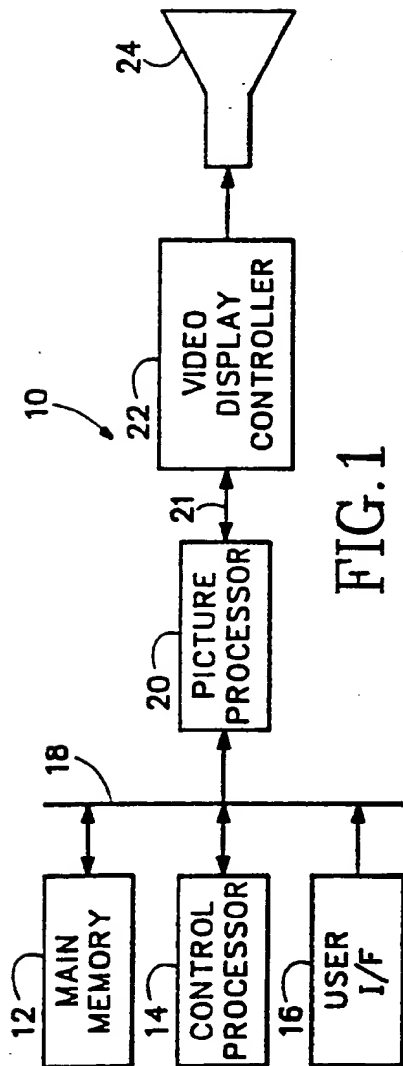


FIG. 1

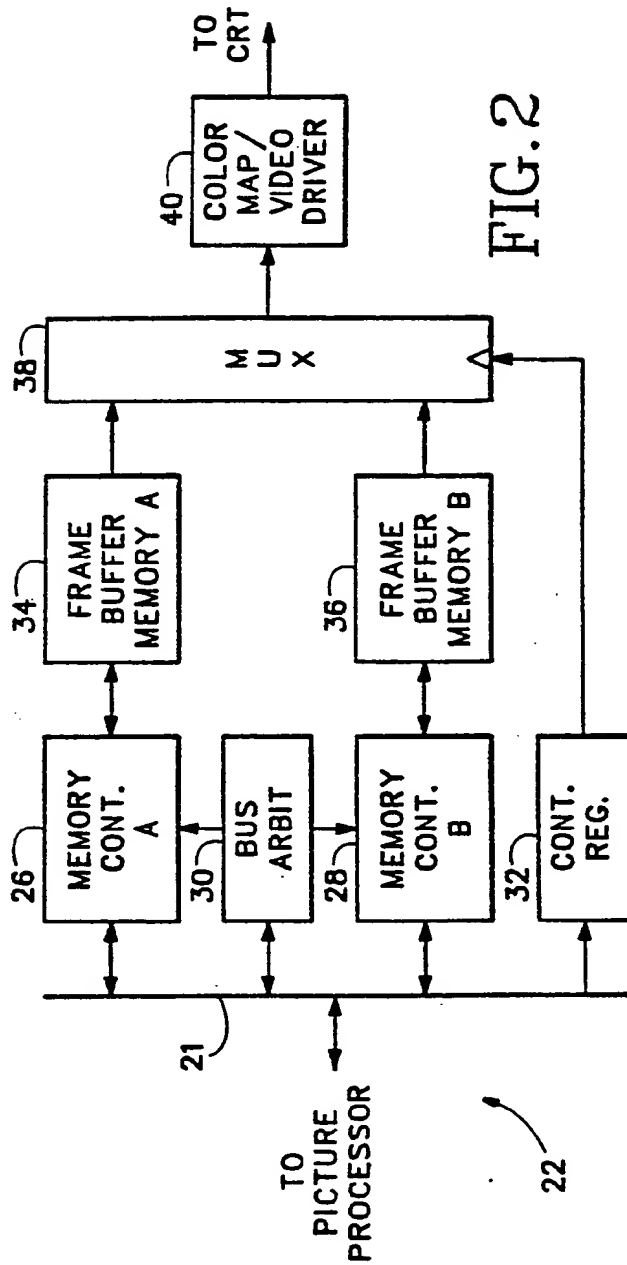


FIG. 2

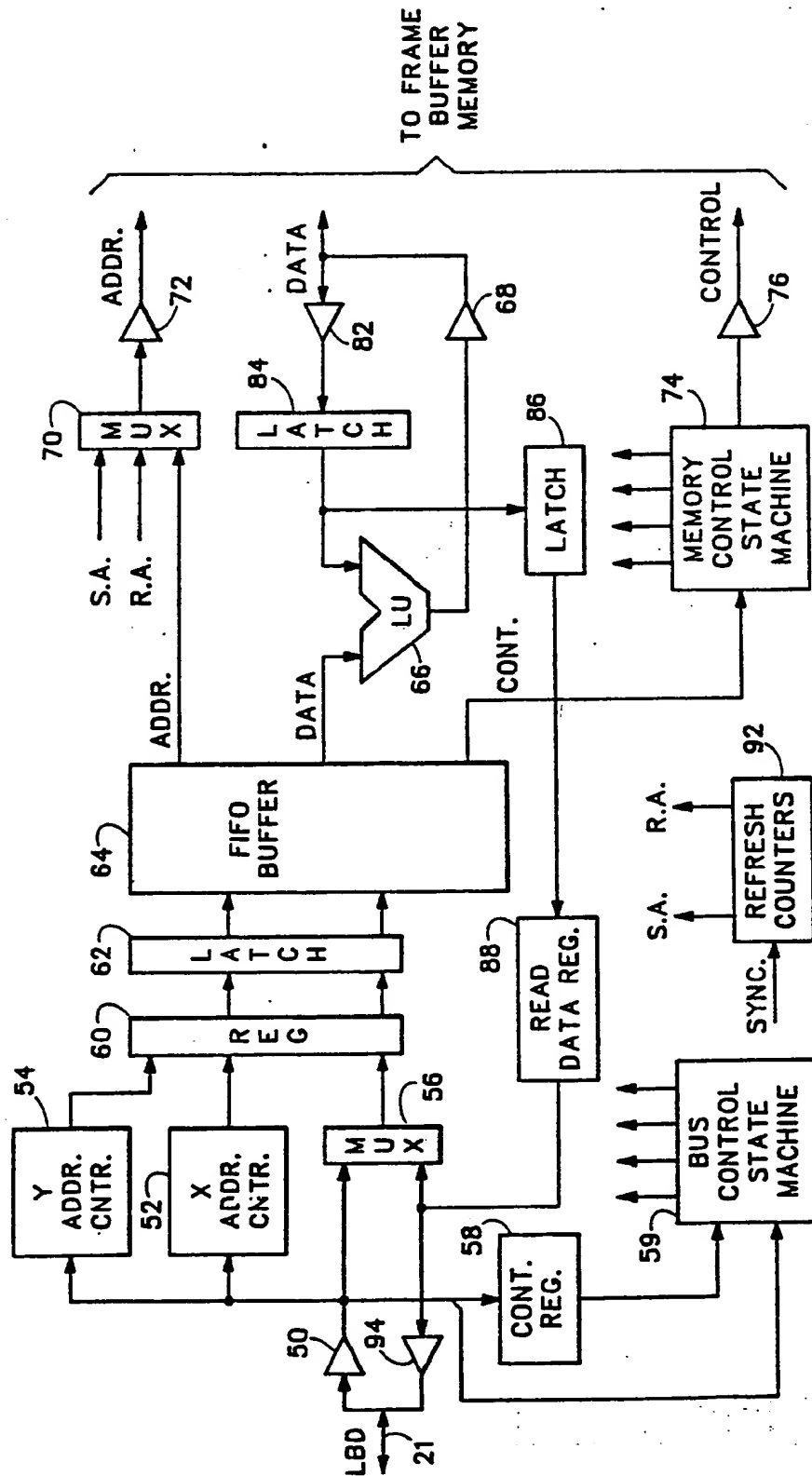
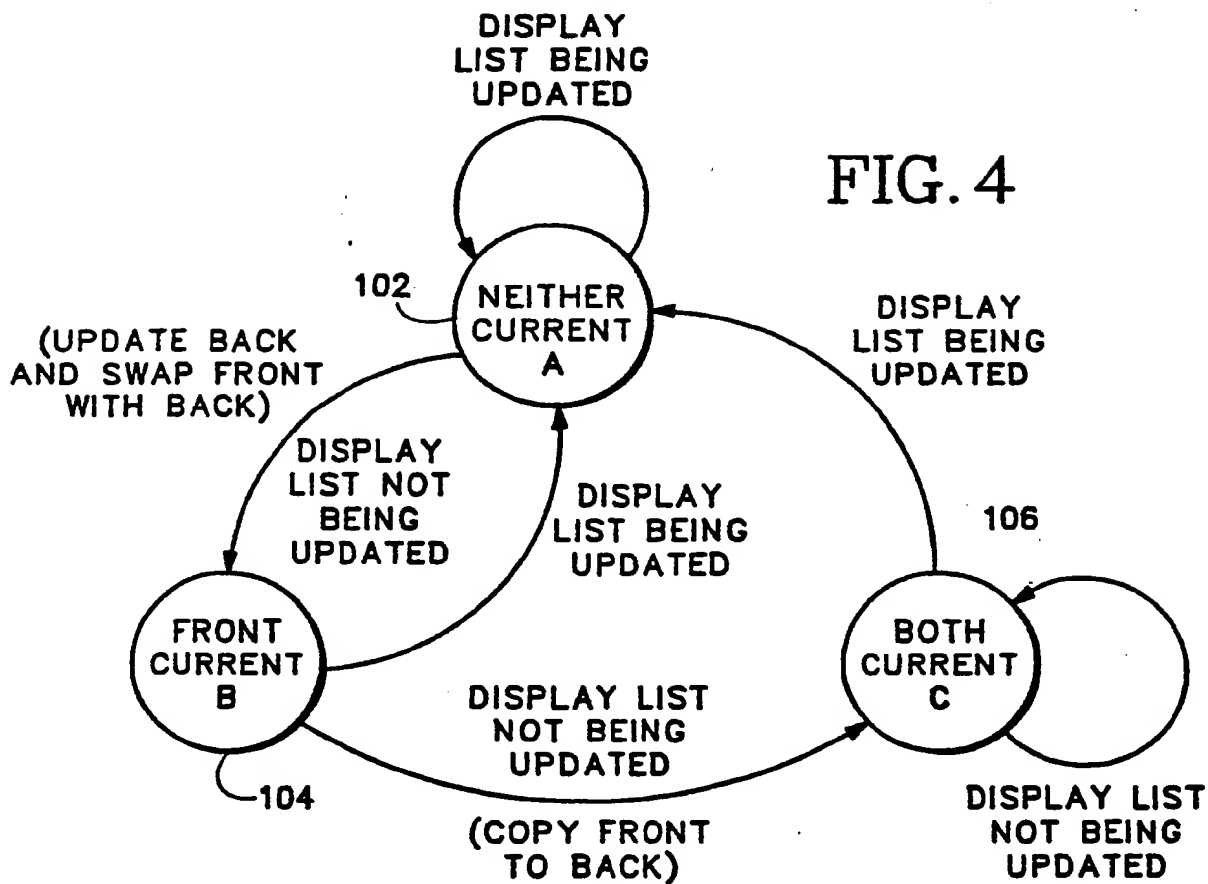


FIG. 3



(19)



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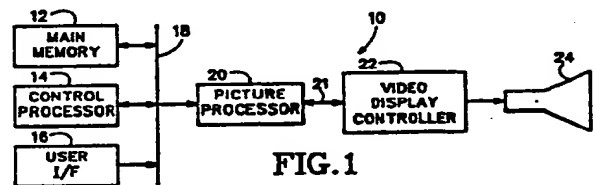
(71) Applicant: TEKTRONIX, INC.
Howard Vollum Park 14150 S.W. Karl Braun
Drive P.O. Box 500
Beaverton Oregon 97077(US)

(72) Inventor: Auel, Kendall Poul
12370 Wilsonville Road
Wilsonville Oregon 97070(US)
Inventor: Delwiche, James Anthony
20898 S.W. 104th Avenue
Tualatin Oregon 97062(US)

(74) Representative: Liesegang, Roland, Dr.-Ing.
FORRESTER & BOEHMERT
Widenmayerstrasse 4
D-8000 München 22(DE)

(54) Double buffered graphics design system.

(57) A graphic display system comprises a video display controller including two similar frame buffer memories for alternatively receiving and storing incoming pixel data and for periodically refreshing a display on a screen selectively in accordance with pixel data stored by either one of the two frame buffer memories. While the video display controller periodically refreshes the screen display in accordance with the pixel data stored in a first of the frame buffer memories, incoming pixel data is stored in the second frame buffer memory. The video display controller begins periodically refreshing the screen display in accordance with the pixel data stored in the second frame buffer memory. Updated pixel data stored in the second frame buffer memory is then copied into the first frame buffer memory.



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European Patent
Office

EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	EP-A-0 231 061 (INTERNATIONAL BUSINESS MACHINES CORP.) * column 3, line 30 - column 5, line 26; figure 1 *	7	G 09 G 1/16 G 09 G 1/28
X	EP-A-0 219 552 (ANRITSU CORP.) * page 7, line 19 - page 11, line 13; figure 1 *	3,7	
A		5,8,10,12	
X	EP-A-0 194 092 (COMPUTER GRAPHICS LABORATORIES INC.) * page 46, line 23 - page 50, line 14; figures 16,17 *	3,7	
A		5,8,10,12	
X	IBM TECHNICAL DISCLOSURE BULLETIN vol. 26, no. 6, November 1983, pages 2906,2907, New York, US; W. HALL et al.: "Low cost, high resolution IBM 3101 Graphics" * the entire document *	7	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
X	EP-A-0 237 706 (INTERNATIONAL BUSINESS MACHINES CORP.) * column 4, lines 36 - column 6, line 7; figure 1 *	7	G 09 G
P,X	EP-A-0 268 687 (FANUC LTD.) * the entire document *	1,2,7	
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 27-02-1990	Examiner KELPERIS K.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

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